

### IN THE CLAIMS

1. (Previously presented) A method of manufacturing a semiconductor integrated circuit, said method comprising:

- forming a device isolation layer in a semiconductor substrate to define first and second active regions;
- forming a plurality of first gate patterns that extend across the first active region and the device isolation layer, regions between the first gate patterns including a first space having a first width and a second space having a second width greater than the first width;
- selectively removing the device isolation layer exposed by the first space;
- forming a line-shaped first impurity region and an island-shaped second impurity region at the surface of the semiconductor substrate exposed by the first space and at the first active region exposed by the second space, respectively;
- forming a second gate pattern that extends across the second active region;
- forming low concentration source/drain regions at the second active region located on both sides of the second gate pattern;
- forming spacers on sidewalls of the second space and on sidewalls of the second gate pattern as well as a spacer layer pattern filling the first space;
- forming high concentration source/drain regions adjacent the low concentration source/drain regions at the second active region;
- removing said spacers to expose the sidewalls of the second space and the second gate pattern and leaving a recessed spacer layer pattern in the first space; and
- forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer pattern.

2. (Original) The method of claim 1, wherein the first active region is defined in a first region of the semiconductor substrate and the second active region is defined in a second region of the semiconductor substrate.

3. (Original) The method of claim 1, wherein the device isolation layer is formed using a trench isolation technique.

4. (Previously presented) The method of claim 1, wherein selectively removing the device isolation layer exposed by the first space comprises:

Amendment After Allowance

Page 2 of 10

Application No. 10/773,805  
Client No. SPX200303-0009US

forming a photoresist pattern that exposes the first space; and  
etching the device isolation layer using the photoresist pattern as an etch mask until  
the semiconductor substrate contacting the device isolation layer in the first space is exposed.

5. (Previously presented) The method of claim 4, wherein forming the first and second impurity regions comprises:  
implanting first impurity ions into the semiconductor substrate exposed by the first space using the photoresist pattern as an ion implantation mask;  
removing the photoresist pattern; and  
implanting second impurity ions into the semiconductor substrate exposed by the first space and the second space using the first gate patterns and the device isolation layer as an ion implantation mask.

6. (Previously presented) The method of claim 1, wherein forming the spacers and the spacer layer pattern comprises:  
forming a spacer layer on the semiconductor substrate having the low concentration source/drain regions, the spacer layer being formed to a thickness which is greater than half of the first width and less than half of the second width; and  
anisotropically etching the spacer layer to expose the second impurity region and the low concentration source/drain regions and to concurrently remain anisotropically etched spacer layer that fills the first space.

7. (Original) The method of claim 6, wherein the spacer layer comprises silicon nitride.

8. (Original) The method of claim 7, further comprising forming a conformal stress buffer oxide layer on the semiconductor substrate having the low concentration source/drain regions before forming the spacer layer.

9. (Original) The method of claim 1, further comprising forming an interlayer insulating layer on the semiconductor substrate having the etching stop layer.

10. (Original) The method of claim 9, wherein the etching stop layer is formed of an insulating layer that has an etching selectivity with respect to the interlayer insulating layer.

11. (Previously presented) The method of claim 9, further comprising:  
patterning the interlayer insulating layer and the etching stop layer to form a first contact hole exposing the high concentration source/drain regions and the second gate pattern;  
patterning the interlayer insulating layer and the etching stop layer to form a second contact hole exposing the second impurity region;  
selectively applying a plug ion implantation process to the second impurity region exposed by the second contact hole;  
forming contact plugs that fill the first and second contact holes; and  
forming metal interconnection lines on the interlayer insulating layer, the metal interconnection lines being formed to cover the contact plugs.

12. (Currently amended) A method of manufacturing a flash memory device, the method comprising:  
providing a semiconductor substrate having a cell array region and a peripheral circuit region;  
forming a device isolation layer in a portion of the semiconductor substrate to define a cell active region in the cell array region and a peripheral circuit active region in the peripheral circuit region;  
forming a stacked gate layer on the cell array region and a peripheral circuit gate layer on the peripheral circuit region;  
patterning the stacked gate layer to form a plurality of stacked gate patterns that extend across the cell active region and the device isolation layer, regions between the stacked gate patterns including first spaces having a first width and second spaces having a second width greater than the first width;  
selectively removing a portion of the device isolation layer exposed by the first spaces;  
forming line-shaped common source regions and island-shaped drain regions at the surface of the semiconductor substrate exposed by the first spaces and at the surface of the cell active region exposed by the second spaces, respectively;

patterning the peripheral circuit gate layer to form a peripheral circuit gate electrode extending across the peripheral circuit active region;

implanting impurity ions into the peripheral circuit active region at a first dose, using the peripheral circuit gate electrode[[.]] as an ion implantation mask, to form low concentration source/drain regions at the peripheral circuit active region;

forming spacer layer patterns filling the first spaces as well as spacers covering sidewalls of the second spaces and also sidewalls of the peripheral circuit gate electrode;

~~forming high concentration source/drain regions at~~ implanting impurity ions into the peripheral circuit active region at a second dose higher than the first dose, using the peripheral circuit gate electrode and the spacer on the sidewall of the peripheral circuit gate electrode as ion implantation masks, thereby providing high concentration source/drain regions;

removing the spacers to expose the sidewalls of the second spaces and the sidewall of the peripheral circuit gate electrode and to concurrently leave recessed spacer layer patterns in the first spaces; and

forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer patterns.

13. (Previously presented) The method of claim 12, wherein forming the device isolation layer comprises:

forming first and second trench mask patterns on the semiconductor substrate in the cell array region and on the semiconductor substrate in the peripheral circuit region respectively;

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a cell trench region in the cell array region and a peripheral circuit trench region in the peripheral circuit region; and

forming a cell device isolation layer in the cell trench region and a peripheral circuit device isolation layer in the peripheral circuit trench region.

14. (Previously presented) The method of claim 13, wherein forming the first and second trench mask patterns comprises:

sequentially forming a gate insulating layer and a lower gate conductive layer on the semiconductor substrate;

patterning the lower gate conductive layer and the gate insulating layer to expose the semiconductor substrate in the cell array region;

sequentially forming a tunnel insulating layer and a lower floating gate layer on the exposed semiconductor substrate;

forming a trench mask layer on the semiconductor substrate having the lower floating gate layer and the lower gate conductive layer, the trench mask layer being formed by sequentially stacking a polishing stop layer and a hard mask layer; and

patterning the trench mask layer.

15. (Previously presented) The method of claim 13, wherein forming the cell trench region and the peripheral circuit trench region comprises:

forming a photoresist pattern covering the cell array region on the semiconductor substrate having the first and the second trench mask patterns;

etching the semiconductor substrate, using the photoresist pattern and the second trench mask pattern as etching masks, to form a preliminary peripheral circuit trench region in the peripheral circuit region;

removing the photoresist pattern; and

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a trench region having a first depth and another trench region having a second depth greater than the first depth in the cell array region and the peripheral circuit region, respectively.

16. (Previously presented) The method of claim 14, wherein forming the stacked gate layer and the peripheral circuit gate layer comprises:

removing the patterned trench mask layer to expose the lower floating gate layer and the lower gate conductive layer;

forming an upper floating gate pattern covering the exposed lower floating gate layer and a first upper gate conductive layer covering the peripheral circuit region; and

sequentially forming an inter-gate dielectric layer and a first control gate conductive layer on the cell array region having the upper floating gate pattern.

17. (Original) The method of claim 16 further comprising forming a metal silicide layer on the first control gate conductive layer and the first upper gate conductive layer.

18. (Previously presented) The method of claim 12, wherein selective removing the device isolation layer exposed by the first spaces comprises:

forming a photoresist pattern exposing the first spaces on the semiconductor substrate having the stacked gate patterns; and

etching the device isolation layer, using the photoresist pattern as an etching mask, to expose the semiconductor substrate that contacts the device isolation layer in the first spaces.

19. (Previously presented) The method of claim 18, wherein forming the common source regions and the drain regions comprises:

implanting first impurity ions into the semiconductor substrate exposed by the first spaces, using the photoresist pattern as an ion implantation mask;

removing the photoresist pattern; and

implanting second impurity ions into the semiconductor substrate in the cell array region, using the stacked gate patterns and the device isolation layer as ion implantation masks.

20. (Previously presented) The method of claim 12, wherein forming the spacers and the spacer layer patterns comprises:

forming a spacer layer on the semiconductor substrate having the low concentration source/drain regions to a thickness greater than half of the first width and less than half of the second width; and

anisotropically etching the spacer layer to expose the island shaped drain regions and the low concentration source/drain regions and to concurrently leave the anisotropically etched spacer layer that fills the first spaces.

21. (Original) The method of claim 20, wherein the spacer layer is formed of silicon nitride.

22. (Original) The method of claim 21, further comprising forming a conformal stress buffer oxide layer on the semiconductor substrate having the low concentration source/drain regions before forming the spacer layer.

23. (Original) The method of claim 12, further comprising forming an interlayer insulating layer on the etching stop layer.

24. (Original) The method of claim 23, wherein the etching stop layer is formed of an insulating layer having an etching selectivity with respect to the interlayer insulating layer.

25. (Previously presented) The method of claim 23, further comprising:  
patterning the interlayer insulating layer and the etching stop layer to form first contact holes exposing the high concentration source/drain regions and the peripheral circuit gate electrode;  
patterning the interlayer insulating layer and the etching stop layer to form second contact holes exposing the island shaped drain regions in the cell array region;  
selectively applying a plug ion implantation process to the island shaped drain regions exposed by the second contact holes;  
forming contact plugs that fill the first and second contact holes; and  
forming metal interconnection lines on the interlayer insulating layer, the metal interconnection lines being formed to cover the contact plugs.

26-39. (Cancelled)

40. (Previously presented) A method of manufacturing a semiconductor integrated circuit, the method comprising:  
forming a device isolation layer in a semiconductor substrate to define first and second active regions;  
forming a plurality of first gate patterns that extend across the first active region, regions between the first gate patterns including a first space having a first width and a second space having a second width greater than the first width;  
forming a first impurity region and a second impurity region at the surface of the first active region exposed through the first space and at the first active region exposed through the second space, respectively;  
forming a second gate pattern that extends across the second active region;  
forming low concentration source/drain regions at the second active region located on both sides of the second gate pattern;  
forming spacers on sidewalls of the second space and on sidewalls of the second gate pattern as well as a spacer layer pattern filling the first space;

Amendment After Allowance

Page 8 of 10

Application No. 10/773,805  
Client No. SPX200303-0009US

forming high concentration source/drain regions adjacent the low concentration source/drain regions at the second active region to provide LDD-type source/drain regions; and  
removing said spacers to expose the sidewalls of the second space and the second gate pattern wherein a recessed spacer layer pattern in the first space remains.

41. (Previously presented) The method of claim 40, further comprising:  
forming a conformal etching stop layer on the semiconductor substrate having the recessed spacer layer pattern.